REMARKS

Claims 1-16 and 19-21 are all the claims pending in the application. Claims 1-16 and 19-21 presently stand rejected. To further clarify the invention, Applicant amends claims 1, 9, 11, and 12. Since the Examiner has already considered these unique features of the claims (*see* page 7 of the Office Action and claims 12 and 20), the amendments do not raise new issues that would require further search and/or consideration.

Preliminary Matter

Applicant thanks the Examiner for returning the initialed form PTO/SB/08 submitted with the Information Disclosure Statement filed on April 29, 2005. Applicant also thanks the Examiner for indicating receipt of the certified copy of the priority document filed with the application on October 19, 2001.

The Examiner has objected to the drawings filed on October 19, 2001 alleging that the drawing is informal. Applicant is submitting herewith one (1) sheet of replacement drawings, which is believed to obviate the Examiner's objection. Acceptance of the replacement drawing is hereby respectfully requested.

Claim Rejection under 35 U.S.C. § 102(e)

Claims 1, 6-12, and 19-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,366,606 to Sriram (hereinafter "Sriram"). Applicant respectfully traverses this rejection in view of the following comments.

Of the rejected claims, only claims 1, 9-12, and 20 are independent. This response initially focuses on these independent claims. To begin, independent claim 1, among a number

of unique features, recites a base station having "one or more digital signal processors, wherein each of said digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing." The Examiner alleges that claim 1 is related to a base station and is anticipated by Sriram.

In particular, the Examiner acknowledges that Sriram discloses different processors for performing the symbol rate processing (symbol rate processor 37) and chip rate processing (correlator co-processor 12), *see* page 7 of the Office Action. The Examiner, however, alleges that having both type of processing be performed by a single digital processor is not considered "an inventive step" (*see* page 7 of the Office Action).

Applicant respectfully submits that "inventive step" is not a standard for a rejection recognized by the MPEP. In fact, to be an "anticipation" rejection under 35 U.S.C. § 102, the reference must teach every element and recitation of the Applicant's claims. Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the reference must clearly and unequivocally disclose every element and recitation of the claimed invention.

For example, in the background of the invention, it is disclosed that a conventional base station has a DSP for performing symbol rate processing and FPGA for performing chip rate processing. The DSP cannot perform the chip rate processing. When speech is transmitted, the data rate is low but the number of users can be high. The speech undergoes the chip rate processing. When transmitting internet data, the data rate is high but the number of users is low. The internet data undergoes the symbol rate processing. The base station should be equipped to

accommodate both situations, when the number of users is high or when the data transmission rate is high. The two situations, however, will never occur simultaneously. Consequently, unused FPGAs or DSPs are always present in the base station. In the present invention as recited in claim 1, however, each digital signal processor can perform a symbol rate processing or a chip rate processing. Thereby, over-dimensioning of the base station is lessened.

Sriram, similar to the conventional technique's described in the background of the invention, discloses a digital receiver 10, which is implemented on a DSP (col. 2, lines 31 to 33). In Sriram, the DSP 10 (the digital receiver) performs the symbol processing using symbol rate processor 37 (Fig. 2; col. 5, lines 51 to 60). The digital receiver, DSP 10 further interfaces with a programmable correlator co-processor 12. The correlator co-processor is not located in the receiver but is a separate unit that communicates with the receiver. It is this correlator co-processor 12 that performs chip rate processing using a chip correlator 34 (col. 2, lines 49 to 54; col. 3, lines 34 to 50). That is, as acknowledged by the Examiner, Sriram only teaches one processor for each type of processing. Sriram fails to teach or suggest a receiver with a digital signal processor that can perform both symbol rate and chip rate processing. In other words, Sriram is no different from the prior art disclosed in the background of the invention.

The Examiner's position can be summarized as follows: two processes can be ran by a single processor as such the present invention as set forth in claim 1 lacks "inventive step" (*see* page 7 of the Office Action). Applicant respectfully disagrees. The Examiner's analysis fails to articulate why these differences would have been obvious to one of ordinary skill. Moreover, Applicant respectfully submits that the present invention recites not just some processes but "a

chip rate processing" and "a symbol rate processing." In the conventional techniques, these two processes require different circuitry. That is, the chip rate processing cannot be executed on any microprocessor but requires special circuitry such as FPGAs or ASICs *e.g.*, correlator co-processor (*see* page 1 of the specification and Sriram). In short, the Examiner's mere allegation that the invention set forth in claim 1 lacks "inventive step" is not grounds for rejection under the MPEP. The Examiner has not set forth any cogent scientific/technical reasoning and/or some objective factual basis to support the Examiner's conclusion that the invention set forth in claim 1 is anticipated by Sriram.

Moreover, at the time the application was filed, assuming *arguendo* that one of ordinary skill in the art would have attempted to implement the chip rate processing on the Sriram's DSP, this would have been at the very least a very inefficient and unreasonable solution, as the base operation for despreading and spreading (complex multiplication of 1 bit by complex values of n bits) could have been implemented only very inefficiently on the Sriram's DSP. Implementing the chip rate processing on the FPGA would have been a much cheaper solution.

Therefore, "one or more digital processors, wherein each of said digital processors is configured to perform a symbol rate processing and at least parts of a chip rate processing," as recited in claim 1, is not disclosed in Sriram, which lacks having a processor configured to perform both types of processing, the chip rate processing and the symbol rate processing. For at least this exemplary reason, claim 1 is patentably distinguishable from (and is patentable over) Sriram. Therefore, Applicant respectfully requests the Examiner to withdraw this rejection of claim 1. Claims 6-8 are patentable at least by virtue of their dependency on claim 1.

Independent claims 9-12 and 20 recites features similar to the features argued above with respect to claim 1. Namely, independent claims 9-12 and 20 recite some variation of a digital signal processor configured to perform a symbol rate processing and a chip rate processing. Claims 19 and 21 are patentable at least by virtue of their dependency on claims 11 and 20, respectively.

In addition, independent claim 20 recites: "means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing, wherein the digital signal processor is disposed inside a receiver." As explained in greater detail above, Sriram fails to teach or suggest having a processor within the receiver with means for performing chip rate processing and means for performing symbol rate processing. In Sriram, the receiver only has a symbol rate processor 37, which does not perform the chip rate processing.

Moreover, in Sriram, there are no switching means as set forth in claim 20. The Examiner alleges that col. 4, lines 35 to 41 of Sriram disclose the switching means set forth in claim 20 (*see* page 4 of the Office Action). Col. 4, lines 35 to 41 of Sriram recite:

> Thus, four cycles are needed to process each symbol. The digital transmissions receiver 10, upon detection of a symbol in the output buffer 38 then proceeds with its symbol rate processing functions. The correlation controller 40 is thus also operable to coordinate processing of and storage of the required chip portions using the addressing information received from the digital transmissions receiver 10 (emphasis added).

In the above-quoted passage of Sriram, however, there are no teachings or suggestion of the switching means that switch from one type of process to another. For at least this additional exemplary reason, claim 20 is patentably distinguishable from Sriram.

In addition, dependent claim 21 recites: "the digital signal processor according to claim 20, wherein the means for switching instructs for transmission of information in the digital processor first to the means for executing chip rate processing and then to the means for executing symbol rate processing." The Examiner alleges that Fig. 2 of Sriram discloses the unique features of claim 21 (*see* page 4 of the Office Action). Applicant respectfully disagrees.

Fig. 2 of Sriram, clearly, does not disclose the order of the processing. Moreover, Sriram only discloses that the digital transmission receiver 10 implements, using symbol rate processor 37, functions such as an overall PN search control during acquisition, finger allocation, time, and frequency tracking, phase correction, combining symbols from the fingers, and some symbol post-processing functions such as de-interleaving and Viterbi decoding (col. 5, lines 50 to 60). However, Sriram fails to teach or suggest having the switching means sending the information first to the chip rate processing means and then to the symbol rate processing means. In fact, Sriram only discloses that the digital receiver communicates with the correlation co-processor 40 during certain time slots (col. 5, line 61 to col. 6, line 4).

In short, Sriram does not teach or suggest the switching means sending the information first to the chip rate processing means and then to the symbol rate processing means. For at least this additional exemplary reason, claim 21 is patentably distinguishable from Sriram.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 2, 3, 13, 14, and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram in view of U.S. Patent No. 4,827,499 to Warty (hereinafter "Warty") and claims 4, 5 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram and Warty, in

view of U.S. Patent No. 6,161,024 to Komara (hereinafter "Komara"). Applicant respectfully traverses these rejections in view of the following comments.

Of these rejected claims 2, 3, 13, 14, and 16, claims 2 and 3 depend on claim 1 and claims 13, 14, and 16 depend on claim 12. Applicant has already demonstrated that Sriram fails to teach or suggest a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing. Warty is cited only for its teachings of processors performing task allocation (see page 4 of the Office Action). Clearly, Warty does not cure the deficient teachings of Sriram. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 2, 3, 13, 14, and 16 dependent upon claim 1 or 12, they are patentable at least by virtue of their dependency.

Moreover, with respect to the dependent claim 3, the Examiner alleges that it would have been obvious to first despread the arriving information and then decode it (*see* page 5 of the Office Action). Applicant respectfully submits that this amounts to a mere conclusory statement and that the Examiner failed to substantiate this allegation with any factual evidence. As explained above, Sriram fails to teach or suggest this unique feature of claim 3. Warty does not cure the deficient teachings of Sriram. For at least this addition reason, dependent claim 3 is patentable over the combined teachings of Sriram and Warty.

Next, the rejected claims 4 and 5, which depend on claim 1, and claim 15, which depends on claim 12, are addressed. Applicant has already demonstrated that the combined teachings of Sriram and Warty fail to teach or suggest at least the digital signal processor configured to

perform a symbol rate processing and at least parts of a chip rate processing, as set forth in the independent claims 1 and 12. Komara is only cited for its teachings of a group of digital processors (*see* page 5 of the Office Action). Clearly, Komara does not cure the deficient teachings of Sriram and Warty. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12, they are patentable at least by virtue of their dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Nataliya Dvorson
Registration No. 56,616

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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